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Lithography Optimization for Sub-22 Nanometer Technologies

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***Abstract*—Continuing scaling of complementary metal-oxide-semiconductor (CMOS) is crucial for the electronic industry because an integrated circuit (IC) with a smaller feature size can provide a smaller silicon area, lower power consumption, higher performance, cheaper price, etc. As the IC process nodes continue to shrink to 22nm and below, the IC industry will face severe manufacturing challenges with conventional optical lithography technologies. According to recent surveys, three most expected technologies may push the limits of lithography: multiple patterning lithography (MPL), electron beam lithography (EBL) and extreme ultraviolet lithography (EUVL). However, each of which encounters different design difficulties and requires solutions for breakthroughs. In this study, we investigate the most critical design challenges of the three technologies: the layout decomposition problem in MPL, the accumulated heating problem in EBL, and the flare effect in EUVL. To overcome these challenges, we transform the original problems into corresponding optimization problems and develop novel algorithms to solve these problems. Experimental results show that the proposed algorithms can efficiently and effectively generate good layout decomposition solutions for MPL, mitigate the thermal problem in EBL, and alleviate flare level and flare variation in EUVL. These results not only can enhance process manufacturability, but also can contribute to the continuing scaling of the CMOS technology.**

I. Introduction

Optical lithography in semiconductor manufacturing is a process that transfers a circuit layout from a photomask to a wafer by exposure to light, as shown in Fig. 1(a). Because an integrated circuit (IC) with a smaller feature size can lead to a smaller silicon area, lower power consumption, higher performance, cheaper price, and so on, continuing scaling of complementary metal-oxide-semiconductor (CMOS) is crucial for the electronic industry [15].

Due to the limitation of the light wavelength used in conventional optical lithography, light diffraction seriously damages printed pattern quality as IC process nodes continue to shrink down. As illustrated in Figs. 1(b) and (c), the pattern can be printed well with a mature process node of conventional optical lithography; however, the pattern could be severely distorted at the 22nm process node and below.

According to the keynote speech at the 2012 International Symposium on Physical Design (ISPD) by Lin (inventor of the immersion process technology), three most expected technologies may push the limits of lithography: multiple patterning lithography (MPL), electron beam lithography (EBL) and extreme ultraviolet lithography (EUVL) [21]. However, each of which encounters different design difficulties and requires solutions for breakthroughs. The three technologies and the most critical challenges are briefly introduced in the following subsections.

A. Multiple Patterning Lithography (MPL)

To overcome the resolution limit of conventional optical lithography, MPL has been regarded as one of most promising solutions,

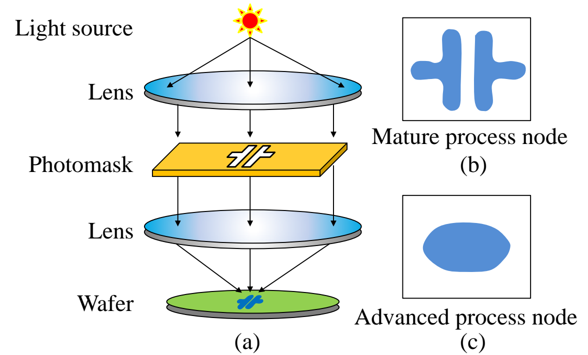

Fig. 1. (a) A conventional optical lithography system. (b) A well-printed pattern at a mature process node. (c) A severely distorted pattern at an advanced process node.

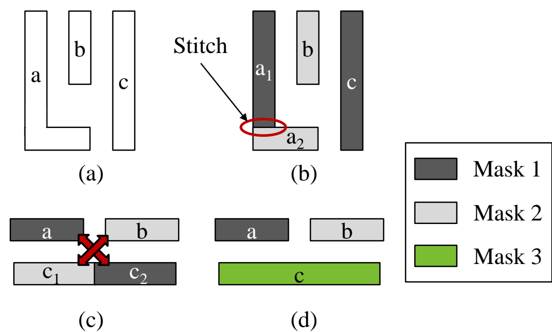

Fig. 2. Multiple patterning lithography. (a) An example layout. (b) Layout decomposition with DPL and an inserted stitch. (c) An indecomposable layout in DPL. (d) The layout is decomposable with TPL.

which uses multiple masks to print each layer of a circuit layout to achieve the goal of pitch relaxation. In MPL, two layout features should be assigned to different masks if their distance is less than the minimum coloring spacing min_{cs}. Otherwise, there will be a *conflict* between these two features. Assigning every feature in a layout to one of the multiple masks is known as *the layout decomposition problem*, whose objective is to minimize the number of conflicts in a decomposition result. To resolve a conflict, a feature may be split into two touching parts and assigned to different masks, which is referred to as *stitch inserting*. An example of double patterning lithography (DPL) is shown in Figs. 2(a) and (b), where the layout can be decomposed into two masks by inserting a stitch.

As DPL has been widely used in industry, triple patterning lithography (TPL) will be required at the 22nm technology node and beyond for gate, contact, and metal-1 layers, which are too complex and dense to be split into two masks [2], [19], [22], [24]. TPL can resolve more conflicts than DPL because of one more mask is

available. As shown in Fig. 2(c), the layout is not decomposable with DPL even if a stitch is inserted. However, this problem can easily be overcome if three masks are available, as shown in Fig. 2(d).

As the DPL layout decomposition problem is usually modeled as a two-coloring problem on a graph, the TPL layout decomposition problem can be modeled as a three-coloring problem. While determining whether a graph is two-colorable and coloring a two-colorable graph can be done in linear time, determining whether a graph is three-colorable and coloring a three-colorable graph are both NP-complete. Thus, the TPL layout decomposition problem turns out to be more complicated and difficult than the DPL layout decomposition problem.

B. Electron Beam Lithography (EBL)

In addition to the conventional optical lithography, there are two most promising Next-Generation Lithography (NGL) technologies: EBL and EUVL. Fig. 3(a) shows an EBL system, where an ebeam is emitted from an electron gun, passes through several lenses and apertures, and directly exposes layout patterns on a wafer. Since EBL is not limited by light diffraction, an e-beam can define very fine, high resolution patterns in a resist. However, high-voltage beams may deposit a considerable amount of heat in a small area and result in critical dimension (CD) distortion [16], [23], [27].

In EBL, patterns are written by beam deflection and stage movement. Since the range of beam deflection is limited, a layout (main field) is split into sub-regions (subfields) and an e-beam writer writes patterns in a subfield at a time [26]. Conventionally, the writing process is usually performed in a sequential manner, as shown in Fig. 3(b). We refer to this as *contiguously sequential writing*: where the writing proceeds in order from one subfield to the next adjacent subfield. However, the contiguously sequential writing process generates heat centralized in a region, which can aggravate the CD distortion problem. To solve this problem, Babin et al. proposed the concept of *subfield scheduling*, which reorders a sequence of the writing process to avoid successive writing of close subfields [1], as shown in Fig. 3(c). Therefore, in a subfield scheduling problem, the objective is to find a labelling (ordering) of subfields where the minimum distance between two subfields with successive labels is maximized.

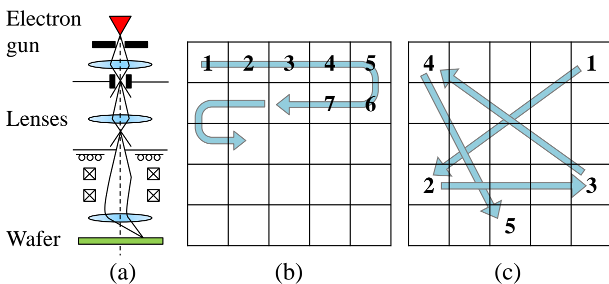

Fig. 3. Electron beam lithography (EBL). (a) An EBL system. (b) The contiguously sequential e-beam writing process. (c) Writing process reordering with subfield scheduling to avoid successive writing of neighboring subfields.

C. Extreme Ultraviolet Lithography (EUVL)

EUVL is also a promising NGL technology because the ten times reduction in wavelength used in EUVL offers the capability of a continuation of Moore's law beyond the 22nm technology node. Fig. 4(a) shows an EUVL system. Since the wavelength of the light used in EUVL is only 13.5nm, the light is absorbed by most of materials. Thus, reflective optical components and masks are used. Due to the surface roughness of the optical system, *flare*, which is undesired scattered light for wafer exposure, becomes one of the most critical issues in EUVL. For the process using a clear-field mask that is also made of reflective materials in EUVL, layout patterns are formed by absorbers on the mask, as illustrated in Fig. 4(b). Thus, during an exposure process on the wafer, the vacant regions not covered by layout patterns will be exposed by the light, and vice versa. However, the scattered flare reduces the contrast between bright regions (vacant regions) and dark regions (layout patterns), and thus flare could result in critical dimension (CD) distortion.

Since flare is proportional to the surface roughness of the optical system and inversely proportional to squared wavelength [25], [31], EUVL suffers from rather high level of flare compared to conventional optical lithography. On the other hand, the regions at the periphery of a chip receive much less flare compared to the regions in the center of a chip (assuming the regions outside the chip boundaries are dark-fields), causing large flare variation within a chip [18]. We refer to the phenomenon as *the flare periphery effect*. In addition, the non-uniformity of layout patterns may contribute to the flare variation as well. For the process with a clear-field mask, regions with lower pattern density contribute to more flare distribution than those with higher pattern density [18], [20]. Since high flare level causes CD distortion and large flare variation damages CD uniformity, flare compensation strategies are required.

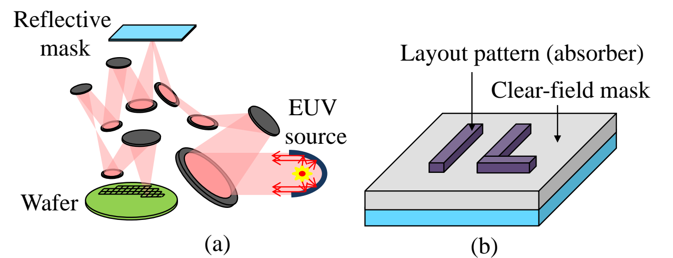

Fig. 4. Extreme ultraviolet lithography (EUVL). (a) An EUVL system. (b) A clear-field mask on which layout patterns are formed by light absorbing materials.

II. Background & Related Work

To tackle the design challenges of the three advanced lithography technologies, previous studies have provided several solutions. In this section, we identify the most critical issues not addressed in the previous studies, thus showing that new algorithms are required for handling these challenges.

A. Layout Decomposition for TPL

Very little research was focused on the layout decomposition problem for TPL. Yu et al. [29] proposed the first systematic study on the general layout decomposition for TPL. Their proposed algorithm extends a stitch-finding method used in DPL to first identify a set of stitch candidates, and then a three-coloring problem is solved by mathematical programming such as integer linear programming (ILP) and semi-definite programming (SDP). The stitch-finding method computes the projections on each feature from its neighboring features within the minimum coloring spacing min_{cs}. Then, a stitch can be inserted at a location where no projection covers. The projection method can find all possible stitch positions in DPL, but we pointed out in [11] that this property does not hold in TPL.

Fig. 5 shows such an example. In the layout depicted in Fig. 5(a), no legal stitch position can be found by using the projection method because all features are covered by projections. Since the layout is not three-colorable, at least one conflict exists after mask assignment, as shown in Fig. 5(b). As illustrated in Fig. 5(c), we can indeed find a legal stitch location and resolve the conflict by inserting a stitch. From this example, we can conclude that not all legal stitch locations can be found by the TPL projection method in [11]; with the previous method, we could miss legal stitches and generate conflicts that can be resolved with stitch insertion.

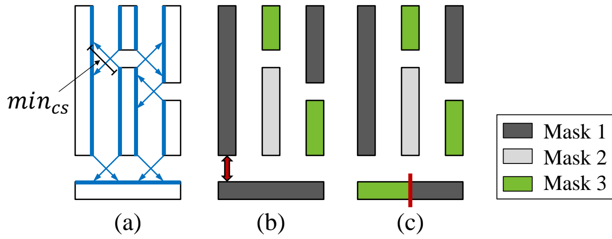

Fig. 5. An example showing that not all legal stitch locations can be found by the projection method in TPL. (a) No stitch location can be found by the projection method. (b) The layout is not three-colorable without stitch insertion. (c) However, a legal stitch location exists and can be used to resolve the conflict.

B. Subfield Scheduling for EBL

The subfield scheduling problem reorders the sequence of the writing process to avoid the successive writing of close subfields. To solve the subfield scheduling problem in EBL, Babin et al. proposed a greedy local improvement method for this problem [1], where a random subfield scheduling is generated at the beginning and the scheduling is iteratively improved by swapping the orders of pairs of subfields. However, there is another important issue in the subfield scheduling problem: the writing process of a subfield can greatly increase the temperature of its neighboring subfields. Those subfields with temperatures higher than a threshold value are called *blocked subfields*: they should not be written in successive writing processes before the temperatures drop below the threshold. As illustrated in Fig. 6, a *blocked box* of a subfield S_i is defined to indicate the block coverage due to the writing process of S_i. To control the temperature better, the time difference between the writing start times of two subfields with overlapped blocked boxes should be as large as possible, which is defined as *the blocked box constraint*. Although the concept of blocked subfields has been proposed in previous studies, no existing work has optimized the subfield scheduling problem while simultaneously considering blocked subfields.

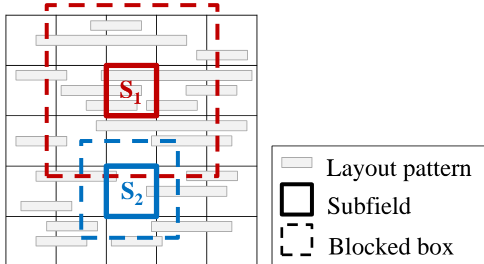

Fig. 6. Blocked boxes for two subfields. The size of a blocked box varies with the pattern density of the corresponding subfield.

C. Flare Optimization with Dummification in EUVL

Dummification (i.e., tiling or dummy fill) is one of the flare compensation strategies to reduce flare level and flare variation in EUVL [18], [28], which inserts redundant patterns in a layout to adjust density distribution. However, existing dummy fill algorithms for Chemical-Mechanical Polishing (CMP) are not adequate for the flare mitigation problem in EUVL due to the flare periphery effect [3], [4], [5], [7], [30]. The objectives of those algorithms mainly focus on density variation minimization or density gradient minimization for a layout. However, the flare variation of a layout with minimized layout density variation could be far from optimal; that is, achieving maximum pattern density uniformity is not equivalent to achieving maximum flare uniformity in EUVL. As shown in Fig. 7(a), a layout with completely uniform layout density distribution may still suffer from large flare variation due to the flare periphery effect. Another layout with smaller flare variation is shown in Fig. 7(b), in which the layout density distribution is less uniform but conforms to the global flare distribution (trend) of the layout. Thus, a more sophisticated dummification algorithm for flare variation minimization in EUVL is required.

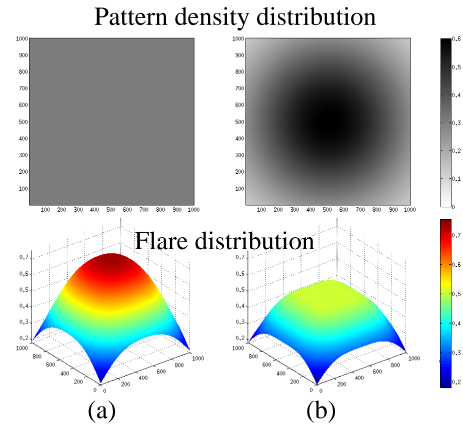

Fig. 7. (a) A layout with uniform density distribution may have large flare variation due to the flare periphery effect. (b) A layout with density distribution conforming to the global flare distribution has smaller flare variation.

III. Approach & Uniqueness

In this section, our proposed algorithms for solving the three problems are introduced. Each algorithm is designed according to the intrinsic property of the problem such that better optimization results can be achieved.

A. Layout Decomposition Algorithm for TPL

As mentioned in Section II-A, since the projection method cannot find all stitch locations in TPL, we do not use this method to find a set of stitch candidates prior to layout decomposition. Our strategy is to first find a good mask assignment solution without considering stitches, and then resolve the coloring conflicts on each mask by inserting stitches [11].

The key part of our layout decomposition flow is a stitch-aware mask assignment algorithm [11]. We first construct a conflict graph to record the geometry relationship among layout features, where a vertex denotes a layout feature, and an edge connecting two vertices if the distance between the two features is less than min_{cs}. Then, we assign a weight to each conflict edge to reflect how hard the corresponding conflict can be resolved by inserting stitches. As illustrated in Fig. 8(a), a larger edge weight indicates that the corresponding conflict is more difficult to be solved by stitches. Having a weighted conflict graph, three independent sets are sequentially found, representing the three coloring classes. Each independent set is found to minimize the total edge weight of the residual graph, as shown in Figs. 8(b)–(d). Finally, each remaining vertex not included in the independent sets is assigned to one of the three sets such that the corresponding conflict occurs at an edge with the smallest weight, as illustrated in Fig. 8(e).

After the coloring, we resolve the coloring conflicts among features by inserting stitches. We first compute the projections from neighboring features on a conflicting feature. See Fig. 9(a) for an example. Then, the conflicting feature can be partitioned into several segments according to the ends of these projections, and these segments have different available colors (masks), as illustrated in Fig. 9(b). Thus, if we can find at least one available color for each segment, then we can solve the conflict by inserting stitches. Then, a plane sweep method scans the conflicting feature from the left to

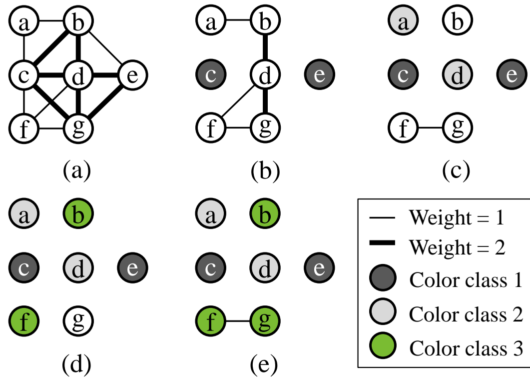

Fig. 8. A stitch-aware mask assignment process. (a) An edge-weighted conflict graph. (b)(c)(d) The constructions of three independent sets. (e) The remaining vertex v_g is assigned to the color class C_3 because the edge weight of e_{fg} is smaller than those of the other adjacent edges of v_g.

the right (or from the right to the left) to find the longest continuous segments, as shown in Fig. 9(c). Finally, as illustrated in Fig. 9(d), we insert a stitch at a suitable location on the feature and assign each segment an appropriate color.

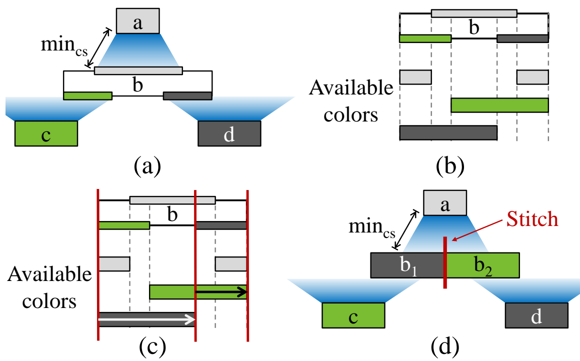

Fig. 9. An example of stitch insertion. (a) Projection computation. (b) Feature partition with the ends of the projections (c) Feature scanning with the plane sweep method. (d) Conflict removal with stitch insertion.

B. Subfield Scheduling Algorithm for Heat Mitigation in EBL

The objective of the subfield scheduling problem is similar to that of the maximum scatter travelling salesman problem (MSTSP), whose objective is to maximize the length of the shortest edge in a Hamiltonian path of a given set of points. Therefore, we transform the original subfield scheduling problem into a constrained MSTSP by additionally considering a blocked box constraint [12].

To tackle the high complexity of the constrained MSTSP, which can be shown to be NP-complete in general, we propose the following methodologies (see Fig. 10) [12]: first, we identify a special case of the MSTSP, in which points are on two parallel lines, and the points on the two lines are aligned. For this special case, we develop a linear-time exact algorithm to efficiently find an optimal MSTSP solution. We then decompose the original subfield scheduling problem into subproblems. Each subproblem is a set of subfields with the same arrangement as the special case, and the blocked boxes are not overlapped with each other to satisfy the blocked box constraint. Finally, each subproblem is solved optimally by applying the linear-time algorithm, and sub-solutions (sub-Hamiltonian paths) are merged into a complete scheduling solution (a complete Hamiltonian path).

Although an optimal MSTSP solution maximizes the distance between any pair of neighboring points in a path, it may cause very close m-neighbors. An m-neighbor of a point p is a point that is at most m points away from p in a path. Close m-neighbors can also incur the heating problem. Thus, we further extend the problem formulation from the MSTSP to the *max-min m-neighbor TSP*, which finds a Hamiltonian path where the minimum distance between any pair of m-neighbors is maximized [14]. To solve the max-min m-neighbor TSP for our subfield scheduling problem, we propose an $O(mn)$-time 2-approximation algorithm for the same special case [14], where n is the number of points, and the same algorithm flow shown in Fig. 10 is used.

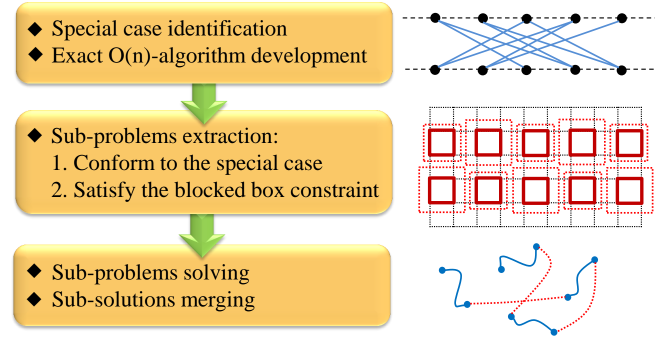

Fig. 10. Our graph-based subfield scheduling flow. We decompose the original problem into subproblems, solve each subproblem independently and optimally, and merge subsolutions into a final scheduling solution.

C. Dummification Algorithm for Flare Optimization in EUVL

As mentioned in Section II-C, a dummification algorithm considering global flare distribution can simultaneously minimize flare level and flare variation. To mitigate the flare effect in EUVL, our key idea is to generate a dummy demand map to guide the dummification process [10].

Flare in EUVL can be modeled as a scattering point spread function (PSF), and a flare map $f(x, y)$ of a given layout can be obtained by convolving the PSF with the vacancy density map $d(x, y)$ of the layout:

$$f(x, y) = d(x, y) \otimes PSF(x, y). \quad (1)$$

A vacancy density map is used since layout patterns are made of light absorbing materials on a mask, and flare is distributed from vacant regions of a layout. Regarding a computed flare map as flare reduction demand, a dummy demand map $D(x, y)$ can be computed by convolving the flare map with a quasi-inverse PSF $Q(x, y)$:

$$D(x, y) = f(x, y) \otimes Q(x, y), \quad (2)$$

where

$$Q(x, y) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} PSF(x - f, y - g)PSF(f, g)df dg. \quad (3)$$

This quasi-inverse PSF models the relation of multiple points on a wafer on one point of the mask. Since the flare of a region can be compensated by inserting dummies into neighboring regions, this quasi-inverse kernel function propagates the flare reduction demand of a region to the dummy demands of neighboring regions. Therefore, the dummy demand of a region is the sum of propagated dummy demands, and thus a dummy demand map can be obtained by convolving the quasi-inverse PSF with a flare map. The illustration of dummy demand map computation is shown in Fig. 11. The larger value of a region in a dummy demand map indicates that the region requires more dummy patterns than those regions with smaller dummy demand values for flare compensation.

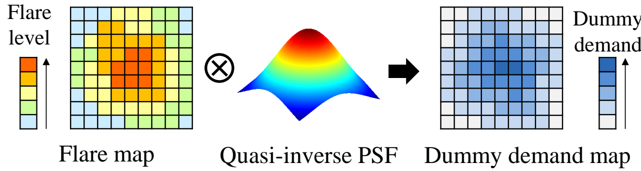

Fig. 11. A dummy demand map can be computed by convolving a given flare map with a quasi-inverse PSF.

IV. Results & Contributions

In this section, experimental results of the proposed algorithms for solving the three critical challenges are reported.

A. Layout Decomposition Results for TPL

We compared the results of our layout decomposition flow with a semi-definite programming (SDP)-based algorithm proposed in the state-of-the-art work [29]. The experiment was based on the ISCAS-85 and -89 benchmarks provided by the authors of [29], and the results are shown in Fig. 12. Averagely, our approach can reduce the number of conflicts in layout decomposition results by 56% with more inserted stitches. The significant improvement in conflict reduction reveals the fact that the previous work only inserts stitches at the locations found by the projection method, and thus some legal stitches are missed, and some resolvable conflicts are generated. In addition, our algorithm flow achieves about 40X speedup, which shows the efficiency of our method compared to the SDP-based algorithm.

B. Subfield Scheduling Results for EBL

To show the effectiveness of our graph-based subfield scheduling flow, we compared our method with a greedy subfield scheduling (GSS) algorithm proposed in the previous work [1]. GSS greedily finds a better scheduling solution by swapping the order of a pair of subfields in each iteration. The experiment was based on the 11 benchmark circuits used in [6], and the maximum temperature of each subfield scheduling solution was computed to show the effectiveness of heating mitigation. The experimental results (see Fig. 13) show that compared with GSS, our approach approximately achieves 30% temperature reduction on average. The substantial improvement may result from the blocked box consideration and the good scheduling solutions generated from our algorithm flow.

C. Flare Optimization Results in EUVL

We compared the flare optimization results between two dummification approaches: (1) a heuristic linear dummification algorithm and (2) our dummification algorithm based on a quasi-inverse lithography technique. To address the flare periphery effect, the linear dummification approach assigns the maximum available dummy value to the central region of a layout and make the dummy values of the farthest regions zero. The MCNC and the industrial Faraday benchmarks were used, and flare level and flare variation were respectively computed. Fig. 14 shows the flare results of original layouts, layouts after linear dummification, and layouts after applying our dummification algorithm. Observed from the experimental results, our algorithm achieves 36% average flare level reduction and 37% flare level variation reduction over the linear dummification approach, showing that our algorithm can effectively alleviate the flare effect in EUVL, and thus the CD uniformity on a layout can be controlled better.

V. Concluding Remarks

In this study, we have provided solutions for solving three most critical design challenges in TPL, EBL, and EUVL. We first transformed the design challenges into optimization problems, and then applied various optimization techniques to elegantly solve these problems. Experimental results have shown that lithography-friendly designs are not only beneficial to lithography performance but also crucial to the development of each advanced lithography technology.

A few top-rated technical conference and journal papers have been published during the development of this research [8], [9], [10], [11], [12], [13], which have attracted much attention in the premier media (e.g., *EE Times* [17]). We believe that these research results have provided key insights into the development of lithography optimization for sub-22 nanometer technologies (and thus have also significantly contributed to the continuing scaling of the CMOS technology).

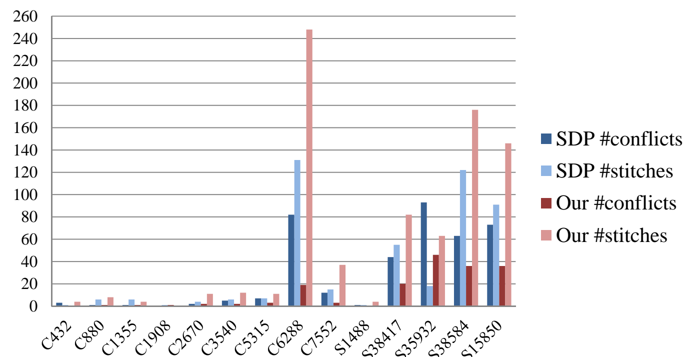

Fig. 12. Comparison of layout decomposition results between the SDP-based method [29] and our algorithm.

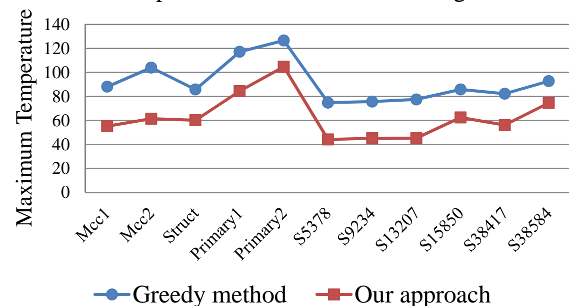

Fig. 13. Comparison of subfield scheduling results between the greedy method [1] and our approach.

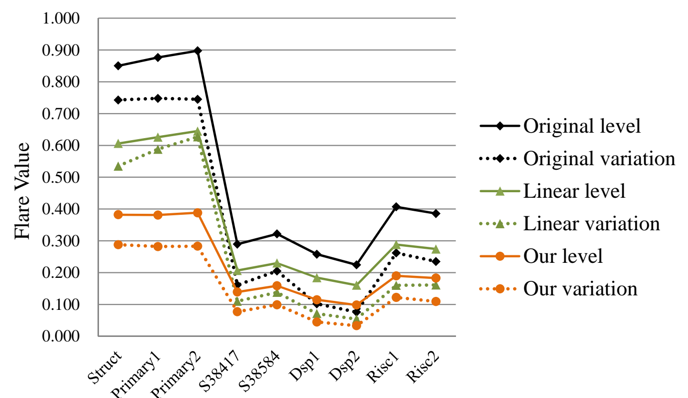

Fig. 14. Comparison of flare level and flare variation among (1) the original layout, (2) a linear dummification method, and (3) our dummification method.

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