ICCAD: G: Toward Unidirectional Routing Closure in Advanced Technology Nodes

Xiaoqing Xu, xiaoqingxu.austin@utexas.edu, ACM ID: 4680577

ECE Department, Univ. of Texas at Austin, Austin, TX 78712

1. PROBLEM AND MOTIVATION

Integrated circuits (ICs) are at the heart of modern electronics, which rely heavily on the state-of-the-art semiconductor manufacturing technology. The key to pushing forward semiconductor technology is IC feature-size miniaturization. However, this brings ever-increasing design complexities and manufacturing challenges to the $350 billion semiconductor industry. The manufacturing of two-dimensional layout on high-density metal layers depends on complex design-for-manufacturing techniques and sophisticated empirical optimizations, which introduces huge amounts of turnaround time and yield loss in advanced technology nodes. Our study reveals that unidirectional layout design can significantly reduce the manufacturing complexities and improve the yield, which is becoming increasingly adopted in semiconductor industry [1, 2]. Despite the manufacturing benefits, unidirectional layout leads to more restrictive solution space and brings significant impacts on the IC design automation flow for routing closure. Notably, unidirectional routing limits the standard cell pin accessibility, which further exacerbates the resource competitions during routing. Moreover, for post-routing optimization, traditional redundant-via insertion has become obsolete under unidirectional routing style, which makes the yield enhancement task extremely challenging. Our research objective is to invent novel CAD algorithms and methodologies for fast and high-quality unidirectional routing closure, which ultimately reduces the design cycle and manufacturing cost of IC design in advanced technology nodes.

2. BACKGROUND AND RELATED WORK

As the technology node scales down to $10nm$ and beyond, unidirectional routing is strongly preferred to provide tight control on lithographic printing for lower metal layers, such as metal-2 (M2) and metal-3 (M3), which complies with underlying self-aligned multiple patterning techniques. However, unidirectional routing is becoming extremely challenging due to sophisticated design rules and high-density routing patterns. This further leads to routing-limited scaling in predictive $7nm$ technology node, which means routing resource competitions are becoming increasingly high, such that design area has to be relaxed to obtain routing closure, i.e. finish all net connections with manufacturing-friendly routing patterns [1].

An example of two-dimensional and unidirectional routing for one two-pin net ($\{a_1, a_2\}$) is shown in Fig. 1[1]. We define preferred routing direction from the top view for M2 and M3 as horizontal and vertical, respectively. Two-dimensional routing means two-dimensional metal patterns are allowed as shown in Fig. 1(a) (top view), where a router connects I/O pins based on wirelength and via minimization, but it is no longer valid due to manufacturability issues in advanced technology nodes. For unidirectional routing in Fig. 1(b) (top view), two-dimensional metal patterns are strictly forbidden and switching routing direction means changing routing layers, which introduces more vias and wirelength. In general, unidirectional routing generates more manufacturing-friendly metal patterns but has more restrictive solution space, compared to the two-dimensional routing.

[1]As a common practice in advanced technology nodes, metal-1 layer is not available for routing due to complex manufacturing constraints.

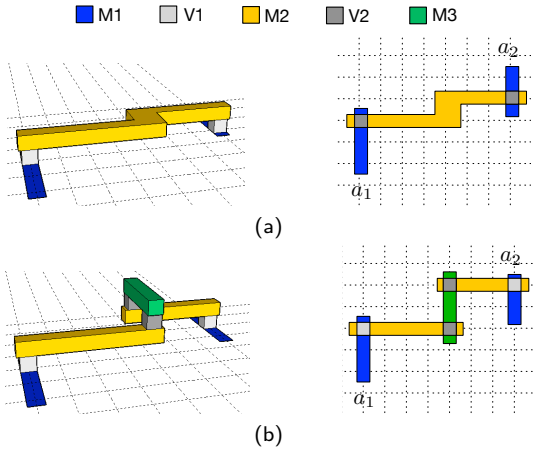

Figure 1: 3D view (left) and top view (right) of (a) two-dimensional routing, (b) unidirectional routing.

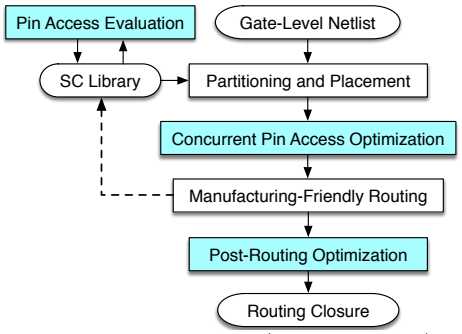

Figure 2: Integrate proposed studies (light blue boxes) into the physical design flow for unidirectional routing closure.

Despite the problem complexities aforementioned, a typical physical design flow for routing closure relies heavily on empirical optimizations in an iterative manner as shown in Fig. 2, which incurs huge amounts of human intervention and turnaround time. Our study identifies the root cause lies in the restrictive solution space from unidirectional routing, which imposes significant impacts on different design stages across standard cell (SC) library design, manufacturing-friendly routing and post-routing optimization. This means a holistic approach is strongly needed to obtain fast and high-quality unidirectional routing closure in advanced technology nodes.

For SC library design, our study reveals that pin accessibility is a major bottleneck for unidirectional routing closure. To improve SC pin access, one simple option is to go through the physical design flow in Fig. 2 using a specific design instance. This would detect "hard-to-access" cells for iterative SC Input/Output (I/O) pin optimizations in a manual procedure as denoted by the dashed line in Fig. 2 [1]. This straightforward approach leads to large turnaround time and design dependency, which motivates the pin access evaluation research for fast and accurate evaluations of SC pin accessibility.

For manufacturing-friendly routing, existing studies follow the

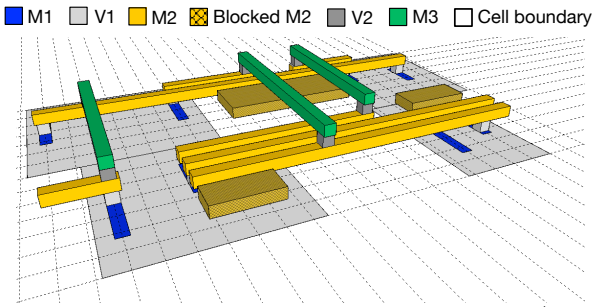

Figure 3: Unidirectional routing for multiple nets on M2/M3 layer.

paradigms of sequential routing [3, 4] or negotiation-congestion-based routing schemes [5,6], which relies on the grid-based search on a routing grid. In general, negotiation-congestion-based routing techniques can resolve routing competitions more effectively than sequential schemes, because a router avoids following a specific net ordering with a history-based heuristic [7]. However, in advanced technology nodes, routing on lower metal layers is becoming more complicated than dealing with manufacturing constraints. An example of unidirectional routing patterns is shown in Fig. 3, which includes multiple pins and nets. Under a routing grid with horizontal and vertical tracks, we observe severe routing resource competitions among multiple nets, especially on M2 layer, where only a small number of horizontal routing tracks overlaps each metal-1 (M1) pin within cell boundaries and one routing track may be shared among different pins [4, 8]. Thus, it is important to globally allocate routing resources among different pins so that all nets can be connected.

In addition, routing resources on lower metal layers, such as M2 and M3, are primarily reserved for short nets. For short-net routing, **via minimization** is particularly important in advanced technology nodes [9]. Furthermore, compared to the previous routing studies [10, 11], unidirectional routing generates a valuable opportunity to explore the solution space using interval-based search instead of grid-based search. This motivates the research for novel approaches to effectively resolve routing resource competitions and enable via minimizations.

For post-routing optimization, redundant-via insertion (RVI) is a widely-adopted approach to improve the manufacturing yield [12]. However, RVI has become obsolete under unidirectional routing style due to inevitable two-dimensional metal patterns. We identify the redundant local-loop insertion (RLLI) as a new way of inserting redundant vias and wires simultaneously to enhance the yield of unidirectional routing [13]. Existing studies on RLLI [13, 14] focus on timing/yield impact evaluations using greedy insertion schemes, without giving globally optimized solutions. This motivates the research for global optimization techniques to achieve better performance than the greedy approach.

The objective of our research is to enable fast and high-quality unidirectional routing closure. Our key contributions are summarized as follows.

- **Fast and accurate pin access evaluation**: We propose a fast and accurate pin access evaluation before a standard cell library is used in a physical design flow, which significantly reduces the turnaround time and design dependency of the traditional approach.
- **From grid-based search to interval-based search**: The unidirectional routing style leads to more efficient interval-based search than conventional grid-based search. We further propose concurrent pin access optimization techniques to efficiently resolve routing resource competitions and enable via minimizations during a routing procedure.
- **Global optimization engine for RLLI**: RLLI emerges as an alternative to RVI for yield enhancement for unidirectional routing. We propose global optimization techniques to generate scalable and high-quality RLLI results.

3. UNIQUENESS OF THE APPROACH

3.1 Standard Cell Pin Access Evaluation

Our study focuses on manufacturing-friendly, standard cell (SC) level pin access design, a priori, before the SC library is used in a physical design flow. We propose the metric of valid hit point combinations (VHPCs) for fast and accurate evaluations of SC pin accessibility. Related definitions are presented as follows.

Definition 1 (Hit Point). The overlap of an M2 routing track (pre-determined by SC architecture) and an I/O pin shape is defined as a Hit Point for that particular I/O pin.

Definition 2 (Hit Point Combination). A set of hit points (with a defined access direction–left or right) where each I/O pin in an SC is accessed exactly once is defined as a Hit Point Combination for that cell.

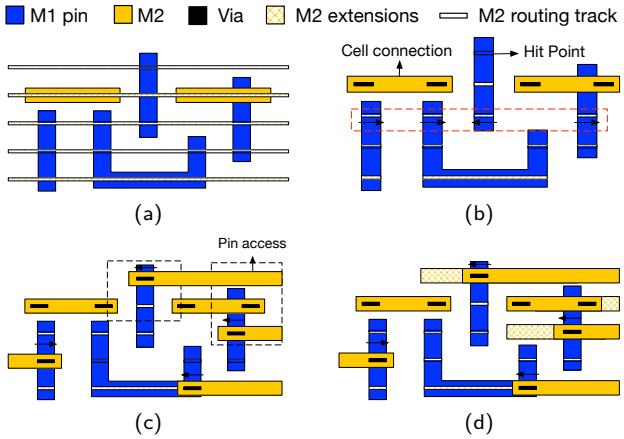

Figure 4: (a) SC I/O pins and M2 routing tracks, (b) hit points and M2 within-cell connections, (c) a hit point combination with M2 pin access, (d) manufacturing-friendly pin access with M2 extensions.

An example of complex SC design is shown in Fig. 4(a), where M2 routing tracks are running horizontally. For each I/O pin, hit points, given by Definition 1, can be extracted from the overlaps of M2 routing tracks and M1 I/O pins in Fig. 4(b). The set of hit points in Fig. 4(c) is a hit point combination, given by Definition 2, where each hit point is associated with one I/O pin. The mainstream industrial routine for SC design has been handcrafted design and optimization. For better pin accessibility, an SC designer mainly focuses on increasing the vertical span of an M1 pin, which provides more hit points for each pin during routing stage [1]. In advanced technology nodes, this technique is becoming less effective due to a small number of M2 routing tracks and pin-to-pin interference [1]. To systematically evaluate pin accessibility under complex pin-to-pin interference, it is important to quantify pin accessibility in terms of "hit point combinations" and "hit points" simultaneously [15]. The number of hit points quantifies the pin accessibility of a single I/O pin in isolation, while the number of hit point combinations evaluates the pin accessibility of entire cell with pin-to-pin interference under advanced manufacturing constraints. Thus, hit point combination provides a more direct metric for designers to optimize I/O pin shapes for better SC pin accessibility.

We further propose pin access and SC layout co-optimization (PICO), an SC library evaluation engine, which provides quick feedbacks of pin accessibility to SC designers. A novel mixed integer linear programming formulation is proposed to determine whether a hit point combination is valid or not based on simultaneous line-end extensions and design rule checks. Thus, the hit point combination in Fig. 4(d) is valid as a legal set of M2 and via patterns can be obtained to access this particular SC.

All possible hit point combinations can be enumerated based on backtracking scheme [15], which generates a compact set of valid hit point combinations. For designers, a robust SC shall provide a maximized number of valid hit point combinations, which can be quickly evaluated by the PICO engine. This further avoids the large turnaround time and design dependency from the traditional approach to detect "hard-to-access" cells.

3.2 Concurrent Pin Access Optimization

We propose track-based routing interval generations for each I/O pin, taking advantage of the unidirectional routing style. Fig. 5(a) enumerates the pin access intervals for pin a_1, which is part of the net containing three pins (a_1, a_2, and a_3). For each I/O pin, a *minimum pin access interval* is the smallest metal strip to cover the pin, while a *maximum pin access interval* is the largest metal strip available within the net bounding box. For pin a_1, we enumerate all the pin access intervals that end at the vertical cutting lines of each diff-net pin, including $I_1^{a_1}$ and $I_2^{a_1}$. We do not enumerate all grids points between a_1 and b_1 because a router has the flexibility to choose any grid point on $I_1^{a_1}$. In Fig. 5(b), those pin access intervals resulting in intra-panel connections shall be preferred in the pin access optimization result, because they connect same-net pins without using external routing resources outside of the panel. This principle of generation enables **interval-based search instead of grid-based search**, which further controls the number of pin access intervals while exactly capturing the pin access interference.

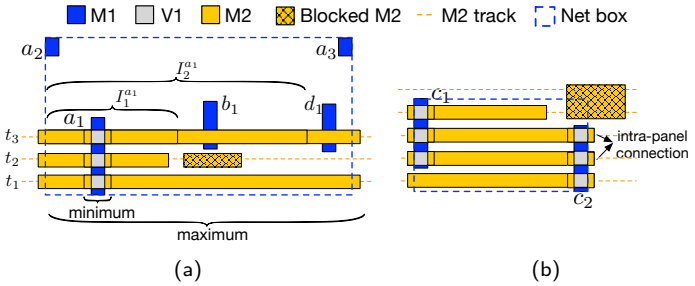

Figure 5: Pin access interval generation, (a) for pin a_1 across 3 tracks, (b) for pin c_1 and c_2 with intra-panel connection.

After track-based pin access interval generation, the pin access intervals may overlap/conflict with each other. The target of conflict detection is to collect all the conflict interval sets on a track without redundancy. In general, this can be realized by generating a vector of intervals and scanning from the left to the right to detect the overlaps. This enables linear conflict set detection, which means the number of conflict interval sets generated is linear to the size of pin access intervals. This principle of conflict detection can significant reduce the number of conflict constraints in the optimization formulation [16].

Among all pin access intervals for all pins, the concurrent pin access optimization is a weighted interval assignment problem, which aims at assigning conflict-free intervals to I/O pins while maximizing and balancing the length of pin access intervals. To obtain the optimal solution of the current pin access optimization, we formulate the weighted interval assignment problem as an integer linear programming (ILP) problem with conflict and selection constraints.

A routing problem may involve millions of pins and nets in advanced technology nodes. To overcome the scalability issue of the ILP formulation, we propose a Lagrangian relaxation (LR)-based approach, which relaxes the conflict constraints to the objective as penalties. A set of Lagrangian multipliers (LMs) is introduced to relax the conflict constraints, while the selection constraints are preserved. As the ILP problem is guaranteed to be feasible, we can obtain a bounded solution to the LR problem during the iterative solving procedure. Each iteration of LR is solved using an efficient greedy algorithm. After obtaining an initial solution, the pin access interval assignments with conflict constraint violations are detected. For any violation, we gradually increase the penalty in the objective by adjusting the corresponding LMs using subgradient descent method [17].

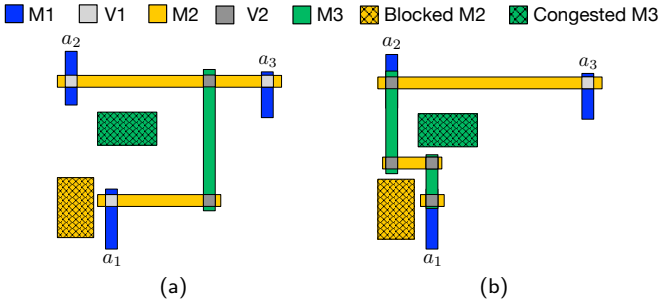

Figure 6: (a) Routing with pin access optimization introducing extra routed wirelength; (b) Routing without pin access optimization introducing extra routed vias.

The routing resource competitions among those pin access intervals from concurrent pin access optimization have been efficiently resolved. Therefore, we implement concurrent pin access router (CPR) to take advantage of these pin access intervals and obtain net connections. The pin access intervals are treated as partial routes connected to its associated pins, which are fed into a negotiation-congestion-based router [6]. As shown in Fig. 6(a), the M2 pin access intervals from pin access optimization are connected to pins a_1, a_2 and a_3. Some detour may happen as M1 pins are connected to pin access intervals (partial routes) on the M2 layer. In Fig. 6(b), the routing results are obtained directly with a negotiation-congestion-based routing scheme. This introduces more vias because the router tries to avoid congested routing regions and routing blockages with unidirectional routing patterns. This means CPR implicitly enables **via minimization** in advanced technology nodes.

3.3 Redundant Local-Loop Insertion

Unidirectional routing style makes conventional RVI (double via) obsolete because unidirectional routing patterns forbid off-track wiring, i.e. wire bending, for the metal coverage of redundant vias. As shown in Fig. 7(a), two redundant vias have been inserted for associated single vias. M2 and M3 tracks are horizontal and vertical, respectively. The redundant via (RV) on the M2 track introduces M3 wire bending and vice versa, which are strictly forbidden under the restrictive unidirectional routing style. Therefore, as demonstrated in Fig. 7(b), redundant local-loop insertion (RLLI), can simultaneously insert redundant vias and redundant wires for yield improvement of unidirectional routing [13]. A redundant local loop (RLL) introduces via and wiring redundancy, i.e. redundant M2/M3 patterns, to guarantee all redundant metal patterns are on-track, which adheres to the unidirectional routing style.

In advanced technology nodes, via density constraints are critical to via manufacturing yield. The windows for via density control are illustrated in Fig. 8. A via layer is partitioned into a set of square regions. Each of the squares has a width of λ and the total number of vias within each window cannot exceed the pre-set upper bound. A possible scenario of the inserted RLLs for neighboring windows, i.e. W_{n+2} and W_{n+3}, is shown in Fig. 8. Under the search space of RLLI, an RLL may cross multiple density windows, such as W_{n+2} and W_{n+3}. This means that the optimal RLLI scheme should simultaneously consider all density windows to globally balance the via densities and maximize the number of RLLs inserted.

The global optimization of RLLI is further formulated into a binary integer linear programming (ILP) problem. We further

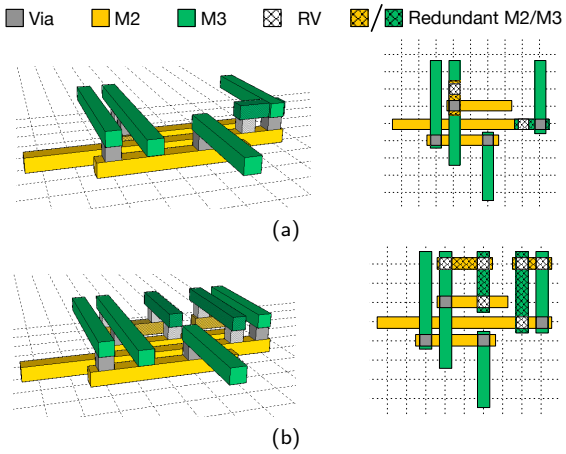

Figure 7: 3D view (left) and top view (right), (a) RVI with wire bending, (b) RLLI for unidirectional routing patterns.

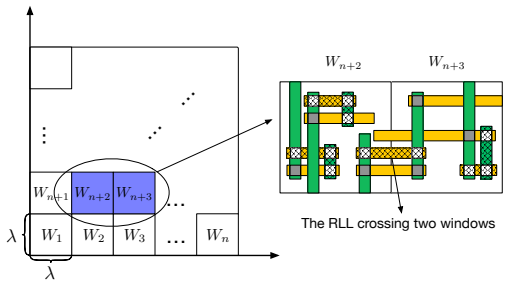

Figure 8: Via density windows.

identify the special constraint structures of the ILP formulation, which leads to a linear programming (LP) relaxation solution that is intrinsically close to a binary solution. Thus, we propose an iterative relaxation and LP solving (IRLS) with incremental search scheme to iteratively solve the LP-relaxed problem instance followed by an incremental search step for a scalable solution. Within each iteration, we determine the integral assignment, ignore non-integer results from the LP solution and update the problem instance. The iteration stops when no integral assignment can be achieved with the LP relaxation for the problem instance. For those single vias without RLLs assigned from the iterative LP solving procedure, an incremental search step is adopted to improve the solution quality.

For the IRLS with incremental search scheme, each iteration of LP solving simultaneously considers all conflict constraints and via density constraints. With an incremental search step, it gives much better solution qualities than the simple greedy scheme. Meanwhile, the LP relaxation leads to polynomial time complexity within each iteration, which makes the runtime of the IRLS with incremental search scheme much more scalable than the optimal ILP approach.

4. RESULTS AND CONTRIBUTIONS

4.1 Standard Cell Pin Access Evaluation

We prototype PICO using ARM 10nm predictive technology library and pin accessibility is quantified by the number of valid hit point combinations (VHPCs) for each standard cell (SC). We compare "PICO" with conventional design rule check ("DRC") in Fig. 9 [15]. For cell-dependent results in Fig. 9(a), "PICO" scheme consistently achieves better performance, i.e. larger number of VHPCs. For "Cell 1", two schemes obtain a similar number of VHPCs, which means manufacturing constraints introduce slight degradations on the pin accessibility. However, the "DRC" scheme achieves 0 VHPC for "Cell 5" while the "PICO" scheme recovers around 200 VHPCs. This means PICO is much more accurate than DRC for pin access evaluation.

To evaluate the library-level benefits, we apply the PICO engine on each cell in the library and illustrate the improvement from PICO over DRC in Fig. 9(b). We quantify the improvement as the "increase of VHPC # in ratio", i.e. the number of VHPCs obtained from PICO divided by that obtained from DRC. The histogram in Fig. 9(b) demonstrates 10X or more improvement in terms of VHPCs for most SCs. For runtime, PICO can be finished within 500 seconds for most cells and within 2 hours for the largest cell. To detect "hard-to-access" cells, PICO is much faster than the traditional approach of synthesizing a design instance through the physical design flow. For fast and accurate pin accessibility evaluation, PICO engine has been prototyped by the leading IP vendor, ARM Inc.

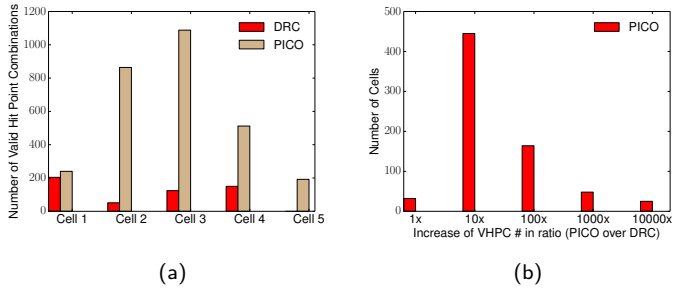

Figure 9: SC pin access optimization using PICO, (a) increase in number of VHPCs for different cells, (b) increase of VHPC # in ratio across the entire library.

4.2 Concurrent Pin Access Optimization

We prototype concurrent pin access router (CPR) using different OpenSPARC modules. We quantify routing solutions with the number of routed nets over the total number of nets ("Routability"), the number of vias ("Via#"), "Wirelength" and "Runtime". "Via#" is the total number of vias for all nets estimated by via per routed net [4]. "Wirelength" is the summation of half perimeter wirelength of unrouted nets and actual grid wirelength for routed nets [4]. High-quality routing results have large "Routability", small "Via#", "Wirelength" and runtime.

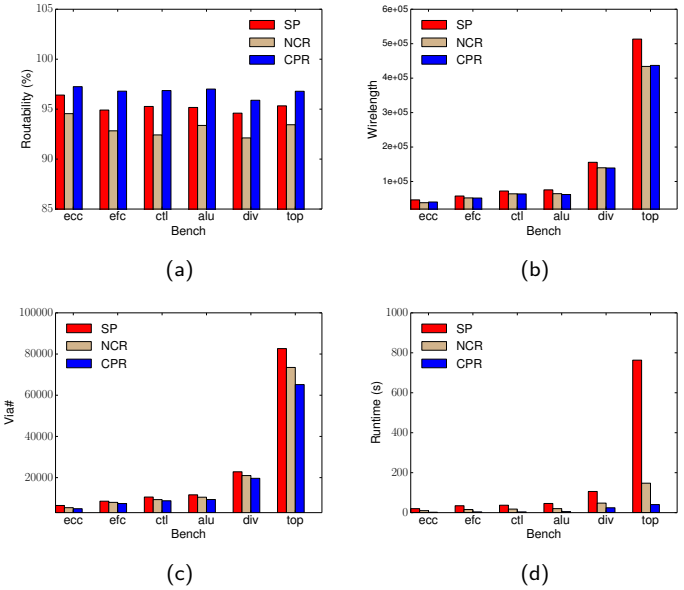

Figure 10: Comparing CPR with conventional routing schemes, (a) routability, (b) wirelength, (c) Via#, (d) runtime.

In Fig. 10, we compare CPR with conventional routing schemes, including sequential pin access planning (SP) [4] and negotiation-congestion-based routing (NCR) [6]. We treat those nets intro-

ducing design rule violations as unrouted nets, which generates design-rule-clean routing results for fair comparisons. Across all benchmarks, CPR obtains the best "Routability", "Via#" and runtime compared to SP and NCR. The CPR reduces "Via#" by $> 10\%$ with negligible "Wirelength" degradations, compared to NGR. This means interval-based search and concurrent pin access optimization represent a new paradigm to resolve routing resource competitions and enable via minimizations.

4.3 Redundant Local-Loop Insertion

We prototype the global optimization engine for RLLI using the unidirectional routing results from [4]. We evaluate the RLLI results in terms of insertion rate, i.e. the percentage of single vias with RLLs inserted over the total number of single vias in a routed design. High-quality RLLI leads to high insertion rate. The IRLS scheme maximizes a weighted sum for global optimization and the greedy approach is adapted from [13, 14]. The IRLS scheme generates much better insertion rate than the conventional greedy approach in a consistent manner across all benchmarks as shown in Fig. 11(a).

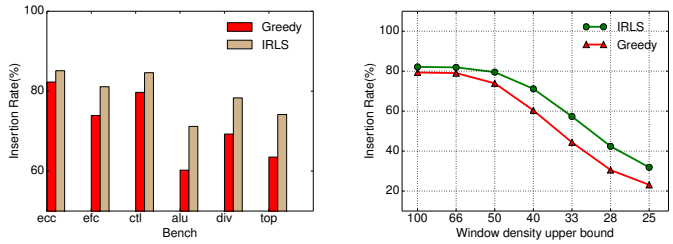

Figure 11: (a) Comparing IRLS with the greedy scheme for RLLI, (b) via density trade-off.

The strength of the IRLS scheme is further demonstrated by the trade-off between the insertion rate and the window density upper bound in Fig. 11(b). The insertion rates are approximately the same for the greedy and IRLS scheme when the upper bound is at 100 due to loose via density constraints. Since the IRLS scheme globally considers the via density constraints in each iteration, we observe better insertion rates when the upper bound is pushed to its lower limit, which represents the typical scenario in advanced technology nodes.

4.4 Research Impacts

My PhD so far has led to **9 first-authored publications** [4, 8, 15, 16, 18–22] in premier EDA/CAD journals and conferences, such as TCAD, TODAES, DAC, ISPD, SPIE etc. Due to strong industrial and academic interests, this study has led to **3 invited papers** [21–23], and my publications have Google scholar citation count 183 and h-index 8, as of April 15, 2017. The PICO engine has been prototyped by the leading semiconductor IP vendor, **ARM Inc**. My research is co-sponsored by Semiconductor Research Corporation (SRC), the world's premier research consortium on semiconductor and related fields. I have received **Best in Session Award** in SRC TECHCON conference 2015. The semiconductor industry is promoting the usage of via pillar (a local-loop structure) for timing and yield enhancement [24]. As technology continues to scale and manufacturing yield becomes more and more critical, we expect increasing industrial impacts of proposed CAD algorithms and methodologies for unidirectional routing closure in $10nm$ node and beyond.

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