1 PROBLEM AND MOTIVATION

Every wireless communication system today, from basic amateur radio operators to large-scale licensed cellular networks, operates in half-duplex (HD) mode — in other words, each wireless device transmits and receives signals either in different time slots (time-division duplexing, TDD) or in different frequency bands (frequency-division duplexing, FDD). Full-duplex (FD) operation relaxes this constraint, allowing for schemes in which the transmission and reception of wireless signals take place simultaneously on the same frequency channel. The realization of FD technology would result in enhanced spectrum efficiency, reduced communication latency, and improved data rates; as a result, it has seen significant attention in literature over the past decade [17].

The primary challenge associated with FD wireless devices is the extremely strong self-interference (SI) signal at the receiver, which requires complete suppression to the noise floor in order to allow for the reception of desired signals. Practically, this requires 70 – 110 dB of SI cancellation (SIC), which is often only achievable through multi-stage cancellation across the antenna, analog, and digital domains [2].

It is challenging to achieve sufficient SIC to enable communication, even at relatively narrow (i.e., ≤ 20 MHz) bandwidths [6]. In addition to the large power differential between the SI and the desired signal, the SI often undergoes substantial frequency dispersion due to long channel delay spreads and is very sensitive to any environmental change, thereby requiring adaptive cancellation.

Programmable Radio-Frequency Integrated Circuit (RFIC) cancellers have been proposed as a means of enabling wideband FD, providing a trade-off between flexibility and complexity [8]. In a previous work [18], we presented a highly-complex programmable RFIC canceller, which leverages sixteen RF taps with variable gain and variable delay to recreate the large SI channel delay spreads with fine resolution. However, even with a suitably capable RFIC canceller, numerous challenges still exist at the system level when developing a full FD radio.

One such challenge is the use of adaptive SI cancellation, necessary when the physical environment surrounding the FD radio is changing [2]. The configuration space of an FD canceller can grow exponentially as the bandwidth increases, thereby requiring computationally efficient algorithms to support wideband RFIC cancellers when deployed in realistic scenarios.

Accordingly, two important challenges that are under-explored in related works are: (i) to design a real-time adaptive controller that enables a highly-complex programmable RFIC to achieve and sustain sufficient SIC even when the physical environment, and therefore the SI channel, is time-varying; and (ii) to integrate the RFIC (along with its real-time controller) into a complete FD radio that is capable of transmitting data over an actual link.

To address these challenges, we present a wideband real-time adaptive FD radio (as shown in Fig. 1) that integrates the RFIC canceller developed in [18] as the front-end of a software-defined radio (SDR). To enable adaptive RF SI cancellation, we developed a two-stage optimization algorithm based on Orthogonal Matching Pursuit (OMP) with Constrained Gradient Descent (CGD); this algorithm is deployed on an FPGA, which computes the optimal configuration to match the SI channel profile as measured by the SDR.

2 BACKGROUND AND RELATED WORK

2.1 Self-Interference Cancellation

SIC can be achieved through a series of combination of different means: at the antenna interface, through analog circuitry, and by digital algorithms.

**Antenna Interface Isolation.** The antenna interface provides passive isolation between the transmit and receive architectures. This can be accomplished through a number...
of means, such as a paired set of transmit and receive antennas [11] or shared antenna interfaces such as circulators [2]. Whereas shared antenna interfaces are preferable for compact form-factor FD implementations, antenna pair configurations can achieve larger bandwidths and higher isolation.

**Analog Cancellation.** Analog cancellation has been proposed through numerous different techniques. Such techniques include (i) amplitude and phase-based cancellers [5], (ii) time-domain cancellers which equalize the delay of the received SI [2], and (iii) frequency-domain cancellers that equalize the spectral components of the SI channel [4].

Recent advances in switched-capacitor capacitor delay lines [18] and N-path filters [14] have enabled wideband implementations of time-domain and frequency-domain equalization approaches that are suitable for small-form-factor RFICs.

**Digital Cancellation.** The antenna interface isolation and analog cancellation stages are crucial in order to prevent the saturation of the receiver’s analog-to-digital converter (ADC), which results in desensitization and renders the radio unable to receive the desired signal. After initially reducing the SI power by these methods to allow for proper digital conversion, the residual SI is then removed through digital SIC. Although each FD radio has perfect knowledge of its intended transmit signal, the presence of nonlinearities and nonidealities in the radio circuitry complicate recovering the SI channel. Many approaches have been proposed to address this challenge, including traditional digital signal processing (DSP) methods [11], hardware modeling methods [16], and machine learning (ML) [10].

### 2.2 RFIC Canceller

In our prior work [18], we developed a switched-capacitor delay-line-based programmable IC (see Fig. 2) that has sixteen RF taps, each with independently configurable gain and delay. The RFIC canceller features three classes of taps, as shown in Table 1: (i) 1 zero-delay, tap in which the input and output are directly connected; (ii) 5 low-delay taps, which provide a delay of up to 2 ns with a resolution of 250 ps and a total of 8 possible delays; and (iii) 10 high-delay taps, which provide a delay of up 8 ns with a resolution of 250 ps and a total of 32 possible delays.

Each tap has a tunable gain with 64 possible values that is enabled by a capacitor-stacking approach to achieve passive voltage gains without noise or distortion penalties [13]. The passive voltage gain is equal to the number of enabled stacked capacitors, thereby allowing us to tune each tap’s individual gain.

The SIC performance of the RFIC canceller depends heavily on its configuration. There are several challenges associated with achieving high SIC, including: (i) the large number ($> 10^{19}$) of possible configurations across the 16 RF taps; (ii) the fact that, due to nonidealities and parasitic effects, the frequency responses of the taps deviate from the ideal model in a practical IC; and (iii) the error incurred from the quantization of the configuration parameters.

### 3 UNIQUENESS OF APPROACH

This section will address our solutions to the two challenges posed in Sec. 1; namely:

1. to develop a real-time adaptive controller that enables a highly-complex programmable RFIC to achieve and sustain sufficient SIC despite time-varying SI channels;
2. to integrate the RFIC and its real-time controller into a complete FD radio system, capable of transmitting data over an actual link.

#### 3.1 Real-Time Adaptive Controller

**Problem Formulation.** We denote the frequency-domain response of the $k$th RF tap with delay setting $\tau_k$ as $H_K(f, \tau_k)$. We can model the frequency response of the RF canceller, across all sixteen RF taps with gains $\{a_K\}$, as

$$H_{RF}(f) = \sum_{K=1}^{16} a_K H_K(f, \tau_k)$$

![Figure 2: Die micrograph of the RFIC canceller [18].](image-url)
In order to maximize cancellation, we want to minimize the residual SI power over a bandwidth $BW$. Given an SI channel $H_{SI}(f)$, then, the cost function for minimization becomes

$$C = \int_{f \in BW} \left| H_{SI}(f) + H_{RF}(f) \right|^2 df$$ (2)

This cost function is quadratic in optimization variables $\alpha_k$ and non-polynomial in $\tau_k$. Instead, if we fix the delays for each tap and consider each tap-delay tuple as a separate tap response, while recognizing that the final configuration can contain at most one tap-delay tuple per tap, we reach the conclusion that this optimization can be simplified to a sparse reconstruction problem.

**Selection of Taps and Delays: OMP.** Sparse reconstructions are a class of problems that utilize an underdetermined matrix (known as the dictionary) of existing signals to find a sparse representation of a signal of interest [7]. For this problem, the dictionary is composed of the measured frequency response for each tap-delay tuple at maximum gain; the signal of interest to be reconstructed is the measured SI channel for any given packet.

To determine the sparse representation, and therefore which taps and delays to select for the configuration, we employ a modified version of Orthogonal Matching Pursuit (OMP). OMP is a low-complexity greedy algorithm which selects the locally-optimal tap-delay tuple in a series of steps, iteratively creating an approximant signal using the dictionary columns and updating the support with a new column in each iteration. Intuitively, our algorithm selects the tap-delay tuple that will maximize the SIC one at a time, and recomputes the approximation using the new selection and appropriate gains.

An important assumptions underlying this measurement-based optimization is that the response of the RFIC canceller is a linear combination of the weighted tap responses. However, this ignores the effects of nonideals in the physical IC, including tap cross-talk and gain nonlinearities; as a result, the measured net response for any given configuration may vary from the expected sum of measured individual tap responses. To minimize these effects, we restrict the number of enabled taps and the net sum of gains across RF taps.

**Gain Adjustments and Tracking: CGD.** After configuring the canceller with the set of selected taps and delays and initial gains, we find that our projected approximation deviates from the measured SI channel. To achieve a more optimal configuration, we iteratively measure this SI residue and adjust the gains using Constrained Gradient Descent (CGD). Specifically, we use a backtracking line search with box constraints on the allowable gain, per the RFIC canceller’s specifications. This method allows us to converge onto an optimal configuration in relatively short order. This process is summarized in Fig. 3.

**FPGA Computation and Configuration.** The algorithm is implemented as a custom hardware image running on an external FPGA. The FPGA receives an instruction code and the most recent SI channel estimate, and in turn computes the optimal configuration using the pre-stored dictionary of tap-delay tuple frequency responses. The selected taps, delays, and gains are then encoded into a 750-bit binary configuration stream, which is transmitted over a Serial-Parallel Interface (SPI) to the RFIC canceller in order to configure the RFIC canceller.

### 3.2 Integrated FD Radio System

**OFDM-Based PHY Layer.** We transmit WiFi-like data packets with a custom Zadoff-Chu (ZC) pilot preamble for robust synchronization and SI channel estimation [9, 12]. The packets consist of pre-generated data modulated using an open-source GNU Radio module for the IEEE 802.11 standard [3]. We then prepend a series of pilot symbols generated using the ZC sequence with cyclic prefix. ZC sequences belong to a class of constant amplitude, zero autocorrelation (CAZAC) waveforms, and are utilized by the 3GPP LTE standard for various functions including reference and synchronization [1]. ZC sequences of length $N$ and root $r$ are characterized [19] by the form

$$b_k = \exp \left( \frac{j \pi k (k + 1) r}{N} \right)$$ (3)

ZC sequences are optimal in the sense that all out-of-phase (non-zero lag) autocorrelation coefficients are zero, thereby allowing for the precise synchronization necessary to accurately estimate the magnitude and phase characteristics of $H_{SI}(f)$.

The SDR transmits and receives at a center frequency of 850 MHz. We experimented with varying bandwidths and transmit powers, as detailed in Sec. 4.
**System Control.** The system is controlled in real time by a custom C++ out-of-tree (OOT) module running in GNU Radio. The controller coordinates across the different operational processes in the GNU Radio flowgraph, and ensures robust synchronization, channel estimation, coordination with the SDR and FPGA, and hardware error recovery. As each packet is received, its pilot symbols are extracted and fed into a linear estimator in order to obtain \(H_S(f)\). The SI channel estimates, with an appended operation instruction, are sent to the FPGA to compute the next canceller configuration. Once the canceller is configured, a new channel estimate representing the residue \(H_S(f)\) is obtained, and the control loop continues until convergence or a set number of iterations is achieved. Additional control mechanisms exist to account for limitations of the hardware due to the high sampling rate requirements.

**Digital SIC.** Time-domain digital SIC is performed on each packet using a least-squares channel estimation (based on the received pilot symbols) and Toeplitz matrix-based convolution [15]:

\[
\mathbf{r}_{\text{RX}} = \mathbf{y}_{\text{RX}} - \mathbf{A}\hat{\mathbf{h}},
\]

where \(\mathbf{r}_{\text{RX}}\) is the residual SI signal after RF and digital SIC, \(\mathbf{y}_{\text{RX}}\) is the residual SI signal after RF SIC, \(\mathbf{A}\) is the Toeplitz matrix constructed from the known transmitted signal, and \(\hat{\mathbf{h}}\) is the SI channel estimated from the pilot symbols.

4 RESULTS AND CONTRIBUTIONS

4.1 Adaptive SIC in Different Environments

We set up the wideband real-time adaptive FD radio for experimentation on a laboratory benchtop and allowed the algorithm to run until convergence, as shown in Fig. 4 for one set of experiments; consistent convergence to a high SIC in only a few optimization steps was observed across all trials.

We recorded the residual SI power at three stages: passive isolation obtained from the antenna interface prior to any active RF SIC, initial cancellation after the coarse-tuned configuration is computed using OMP, and the optimal cancellation achieved during the fine-tuning stages using CGD. Figure 5 shows the total RF cancellation at each of these three stages across four different bandwidths, ranging from 10 MHz to 100 MHz, sweeping across transmit powers from -10 dBm to 0 dBm.

It was found that increasing transmit power did not have a large impact on the RFIC canceller’s optimal performance; however, as bandwidth increased, performance dropped. The total time necessary for the initial tap selection via OMP is approximately 0.5 sec and each subsequent adaptive CGD step takes approximately 0.3 sec.

These experiments were repeated with the FD radio enclosed by heavy steel plates, creating a strong environmental blocker and therefore changing the initial SI channel. Despite this change, similar performance was achieved, as shown in Fig. 6. As in the previous experiments, increasing bandwidth decreases the RFIC canceller’s optimal performance.

4.2 Adaptation During Mobility

We extended our exploration of the environmental adaptation capability by integrating the FD radio into a mobile node and moving it along a pre-determined path with different environmental conditions along the way, as shown in Fig. 7.

The configuration was continuously tracked and updated every three meters by CGD, and resulted in a consistent...
Figure 7: FD radio deployed as a mobile node, overlayed onto the path taken. Measurement points are highlighted in green.

Figure 8: Five different configuration profiles were selected by the controller as the cart moved along the hallway. Whenever the RFIC canceller’s performance dropped, a complete reconfiguration was performed to return to previous performance levels.

SIC of 50 dB across antenna interface isolation and RFIC cancellation. Whenever there was a significant drop in SIC performance, a full recomputation (including OMP for new tap-delay tuple selection) was performed to return to the baseline previous performance, as shown in Fig. 8.

REFERENCES


